REMARKS

At the time of the Final Office Action dated May 20, 2003, claims 1-18 were pending in this application. Of those claims, claims 1-5 have been rejected. Applicant acknowledges, with appreciation, the Examiner's allowance of claims 6-18. Claim 1 has been amended, and claims 8-12 have been cancelled. Care has been exercised to avoid the introduction of new matter. Specifically, claim 1 has been amended by incorporating the limitations of allowable claim 8 therein, and consequently claim 8 has been cancelled. Applicant submits that the amendment to claim 1 does not raise any new issues not already considered by the Examiner.

Claim 1 is rejected under 35 U.S.C. § 102 for lack of novelty as evidenced by Hasegawa, JP 6-50824

In the third enumerated paragraph of the Office Action, the Examiner asserted that Lee discloses a semiconductor device corresponding to that claimed. As claim 1 has been amended to include allowable claim 8, Applicant submits that Examiner's rejection has been traversed.

Claims 2-5 are rejected under 35 U.S.C. § 103 for obviousness based upon Hasegawa in view of Jain et al., U.S. Patent No. 6,107,165

In the fifth enumerated paragraph of the Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the semiconductor device of Hasegawa in view of Jain to arrive at the claimed invention. As claim 1 has been amended to include allowable claim 8, upon which claims 2-5 ultimately depend, Applicant submits that Examiner's rejection has been traversed.

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

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Version with markings to show changes made

IN THE CLAIMS:

1. (Twice Amended) A semiconductor device comprising:

a substrate;

a first interconnection formed on said substrate;

a first dielectric film covering said first interconnection;

an opening section extending from a surface of the first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed over said plug;

a predetermined void between said plug and said second interconnection; and

a second dielectric film covering said second interconnection, wherein said predetermined void separates said plug from said second interconnection.

6. (Twice Amended) A semiconductor device comprising:

a substrate;

a first interconnection formed on said substrate;

a first dielectric film covering said first interconnection;

an opening section extending from a surface of said first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed on said first dielectric film in the vicinity of said plug ;

a second dielectric film covering said second interconnection; and

a predetermined void in said second dielectric film and located at a position adjacent to said second interconnection and at a position directly over and above said plug.